25.6 A 92.5mW 205MS/s 10b Pipeline IF ADC Implemented in 1.2V/3.3V 0.13µm CMOS

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The performance of a pipeline ADC is strongly connected to accuracy of the gain of each pipeline stage. This gain depends on both capacitor mismatch and finite opamp open-loop gain. In modern CMOS technologies the capacitor matching is fulfilled when capacitors are dimensioned according to SNR requirements. Further, to reach the speed specification of the ADC, the core digital transistors must be used. Due to the low supply voltage, more complex opamps are required [1] to fulfill the open-loop gain requirement, increasing both power dissipation and die area. The ADC presented in this paper uses simple single-stage opamps throughout the pipeline chain, adjusting for the low opamp gain by continuous background calibration. A drawback with such calibration is the long update time of the calibration coefficients, increasing the startup time of the converter dramatically. This is solved by using foreground calibration at start up, and thereafter continuous background calibration covering long-term gain variations due to temperature variations and aging. A broadband low-distortion buffer and a THA are preceding the ADC to take care of IF/RF sampling. The ADC and THA are running at 1.2V supply while the input buffer is using 3.3V. The ADC is designed for 205MS/s sample rate and 300MHz ERBW. The ADC consumes 92.5mW from both supplies, 9.0 ENOB for signal frequencies up to 100MHz and 8.5 ENOB at 330MHz.

Figure 25.6.1 shows the low-distortion voltage buffer and the THA preceding the ADC. The voltage buffer is necessary to ease the off-chip driving requirements of the THA. The buffer is based on an ordinary source follower with the drain of MN_{SF} connected to the positive supply, and the gate of MN_S biased with a fixed voltage. Such voltage follower has signal attenuation and generates too much distortion for 10b performance, even at low signal frequencies. The finite output resistance of MN_S and MN_{SF} is highly nonlinear due to the large swing of their drain-source voltages. MP_{SF} and MP_S are added, acting as an additional voltage follower. The drain and source voltages of MN_{SF} will now track each other, and the effect of the finite and nonlinear output resistance of MN_{SF} is eliminated. Further, by using the current through MP_{SF} as bias current for MN_{BS} (and the gate-voltage of MN_S) a feedback loop is added. The feedback loop measures changes in the MN_{SF} current and feeds it back through MN_S. This increases and linearizes the drain-source resistance of MN_S, and reduces the current variation through MN_{SF} over the voltage swing. The result is lower attenuation and distortion in the whole frequency range of the buffer. The buffer input common-mode (CM) voltage is set of the desired CM-voltage at the input of the THA, adjusted for variations in the threshold voltage of MN_{SF}. The complete voltage buffer draws 4.3mA from the 3.3V supply. The THA has the flip-over structure. The signal voltage is applied over the C_H capacitor in the ϕ_1-phase, and in the ϕ_2-phase C_H is connected around the Miller OTA. Both ϕ_1- and ϕ_2-switches are bootstrapped, while the sampling switch, controlled by ϕ_{1B} (the early clock of ϕ_1), is a PMOS-switched-N-well type [1].

To keep the performance of a pipeline ADC at 10b level, the open-loop gain of the stage opamp has to be above ~70dB. To obtain such gain in modern low-voltage CMOS technologies, 2-stage opamps are needed. These opamps require extra die area and current consumption because of the compensation capacitors that are even larger than the stage sampling capacitors. Therefore, this design uses single-stage 25dB open-loop gain opamps only. This results in reduced stage gain, that is digitally calibrated for [2]. An overview of the ADC is shown in Fig. 25.6.2. The pipeline consists of 8 dithered pipeline stages (DPS) that each are calibrated individually, and a backend ADC consisting of three 1.5b stages and a 2b flash at the end. The calibration scheme can be divided in 2 parts. At startup of the converter, 211 clock cycles are used to do foreground calibration of the ADC [3]. This is done by enabling the CAL-startup block. CAL-startup applies a test signal at the input of each stage, beginning with the last calibrated stage. The gain of the 8th stage and the backend ADC is now measured and the gain coefficient of this stage is computed. This procedure is then repeated sequentially from 7th to 1st stage, computing one calibration coefficient for each stage. When finished, the ADC enters the continuous background calibration mode. A dither signal is injected in the analog signal path in each stage. The same dither signal is subtracted digitally such that the digital output of the converter does not contain the dither if the calibration coefficients are correct. The COR-block measures the leakage of the dither at the ADC output by correlating the output by the injected dither. The gain coefficient is updated such that this leakage is minimized. The gain coefficients are implemented in the vertical branches below each stage. Since the digital stage output is either of {-1, 0, 1}, the multiplications with the gain coefficients can be done by additions, avoiding costly multipliers when running in background calibration mode. Further, due to the reduced gain throughout the pipeline chain, the signal experiences some compression. This effect results in missing codes when multiplied with the gain coefficients. To obtain no missing codes at 10b level, the resolution of the pipeline is increased to 13b internally by adding 3 heavily downscaled stages at the end of the pipeline chain.

The DPS is shown in Fig. 25.6.3 and is an ordinary 1.5b stage [1] with some modifications to implement the calibration. At startup (START=1), the gain of the stage is measured. In the sampling phase (ϕ_1), zero signal is measured across the sampling capacitors C_1 and C_2. In the hold phase (ϕ_2), the stage output is spanned out by applying a test signal at the top of C_1. The value of the test signal is the reference voltage, and the sign is altered by the dither signal TS. In continuous calibration mode START=0 and the dither signal is applied by connecting C_t to either V_{REFP} or V_{REFN} according to the dither signal TS.

Figure 25.6.4 shows that the SNDR remains flat for sampling rates from 10 to 205MS/s ($F_{IN}=F_S/2$), and drops by 4dB at 300MS/s. The ADC scales its power dissipation automatically with the applied clock frequency [1, 4], achieving an efficient converter at any sampling rate. Figure 25.6.5 shows the performance versus signal frequency. The SNDR starts out at 56dB at low frequencies, it is above 55dB up to 200MHz, and rolls off to 53dB at 330MHz. SFDR remains above 60dB up to 330MHz. Up to 200MHz SFDR is limited by odd harmonics, mainly due to the accuracy level of the calibration coefficients. Above 200MHz SFDR is limited by second harmonic, caused by poor symmetry in the off-chip signal transformer. Figure 25.6.6 summarizes the key parameters of the ADC and Fig. 25.6.7 shows the die micrograph. The active die area is 0.52mm^2.

References:

[1] B. Hernes, A. Briskemyr, T. N. Andersen, et al., "A 1.2V 220MS/s 10b Pipeline ADC Implemented in 0.13µm Digital CMOS," *ISSCC Dig. Tech. Papers*, pp. 256-257, Feb., 2004.

[2] E. Siragusa, I. Galton, "A Digitally Enhanced 1.8-V 15-bit 40-MSample/s CMOS Pipelined ADC," *IEEE J. Solid-State Circuits,* vol. 39, Dec., 2004.

[3] J. Bjørnsen, "Method and Apparatus for Start-Up of Analog-to-Digital Converters," *United States Patent No. US 6,970,120 B1*, Nov. 29, 2005.

[4] T. N. Andersen, B. Hernes, A. Briskemyr, et al., "A Cost-Efficient High-Speed 12-bit Pipeline ADC in 0.18µm Digital CMOS," *IEEE J. Solid-State Circuits,* vol. 40, pp. 1506-1513, Jul., 2005.

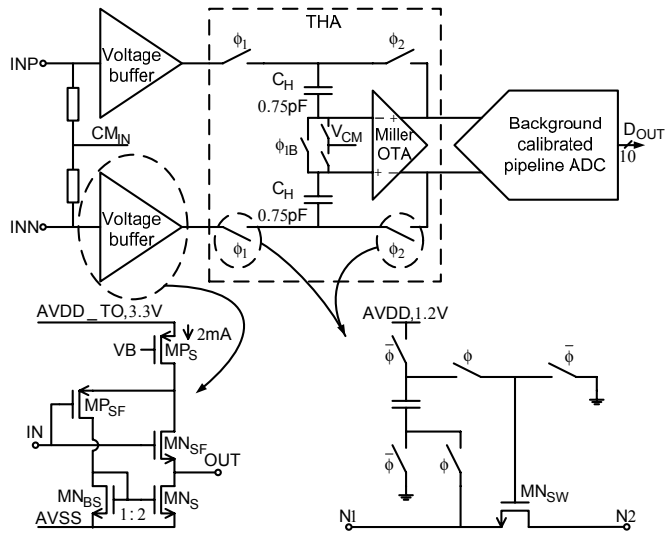

Figure 25.6.1: ADC with broadband input voltage buffer and THA.

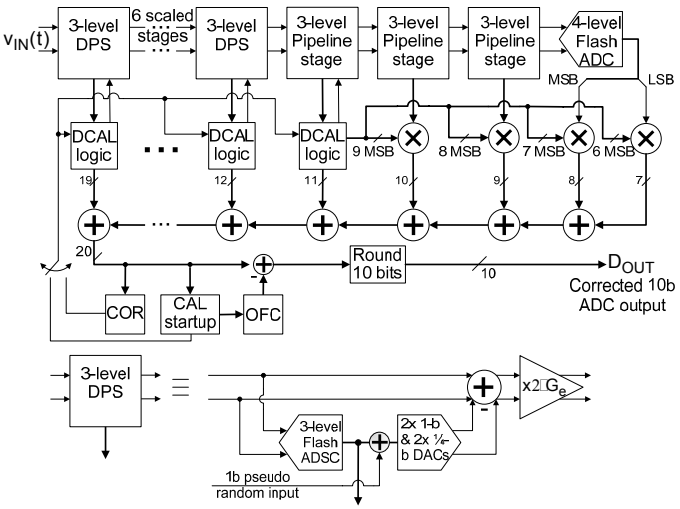

Figure 25.6.2: Digital calibrated ADC.

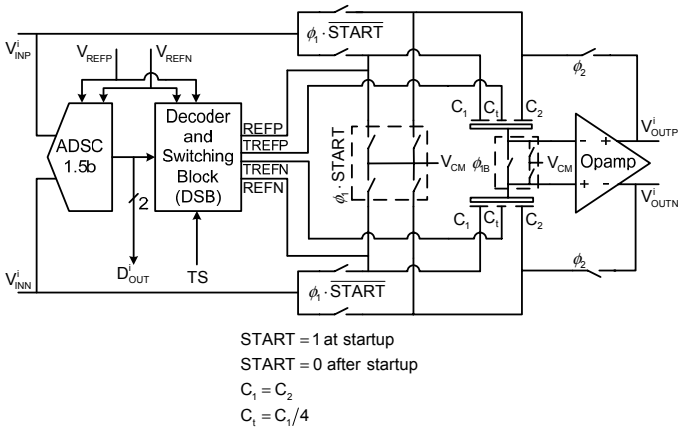

Figure 25.6.3: 1.5b dithered pipeline stage.

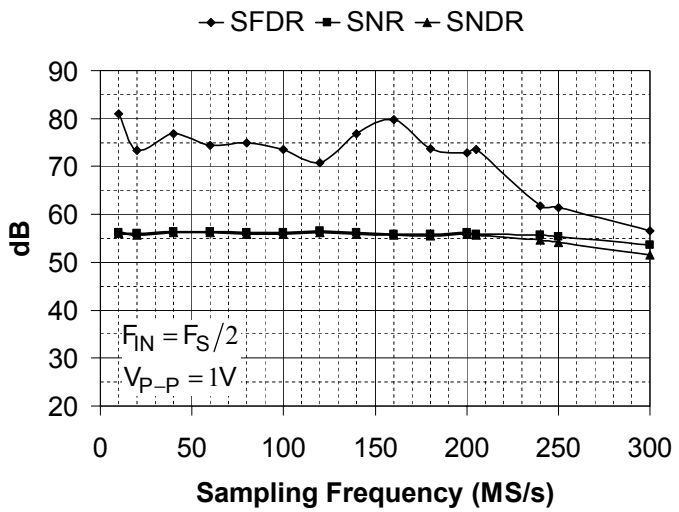

Figure 25.6.4: Performance versus sampling frequency.

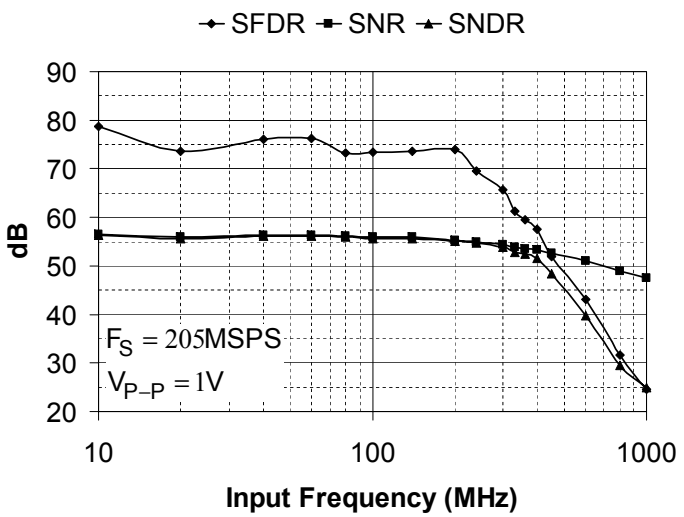

Figure 25.6.5: Performance versus input frequency.

Technology	0.13µm digital CMOS + deep N-well and low VT
Supply Voltage	1.2V/3.3V
Resolution	10b
Sampling frequency, F_S	205MS/s
Full-Scale analog input	1.0 V_{PP}
Die area	0.52mm^2
Power 3.3V supply (buff.)	14.2mW
Power 1.2V analog	67.5mW
Power 1.2V digital	10.8mW
Tot. power dissipation	92.5mW
DNL/INL	±0.15 LSB /±0.6LSB
SFDR (f_{IN}=F_S/2)	73.5dB
ENOB (f_{IN}=F_S/2)	9.0b
ERBW	330MHz

Figure 25.6.6: Key measured results.

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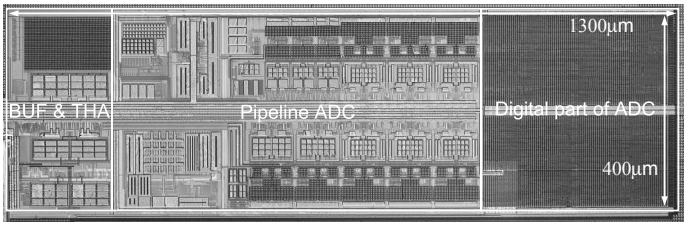

Figure 25.6.7: Die Micrograph.

